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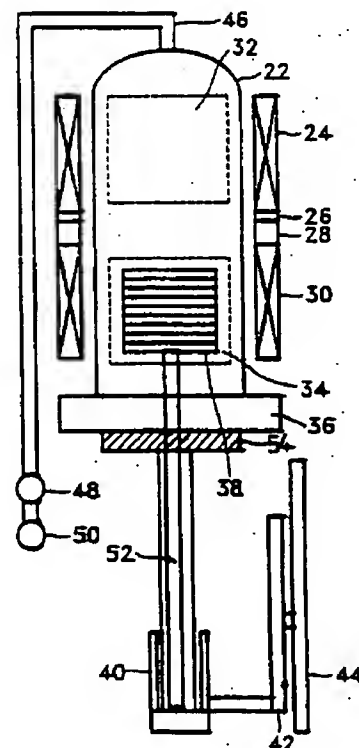
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(54) Apparatus for rapid thermal processing

(57) An apparatus for rapid thermal processing comprises a furnace in vacuum state, a first heater (24) which is located at an upper part of the furnace and has an annular shape surrounding the furnace, and a second heater (30) which is located at a lower part of the furnace vertically below the first heater (24), and also has an annular shape surrounding the furnace. A reflector (26) and a heat shield (28) help to ensure an abrupt temperature change in the vertical direction. As a result, overheating of the wafer beyond a required temperature can be prevented, thereby decreasing the thermal budget. Also, the temperature distribution over the whole wafer can be evenly maintained, thereby preventing the generation of slip. Furthermore, a shallower junction than with the general furnace can be obtained.

FIG. 2



A search has been completed on amended claims filed 8/3/96 which were amended in response to an objection under s.76(1).

The date of filing shown above is that provisionally accorded to the application in accordance with the provisions of Section 15(4) of the Patents Act 1977 and is subject to ratification or amendment.

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FIG. 1
(PRIOR ART)

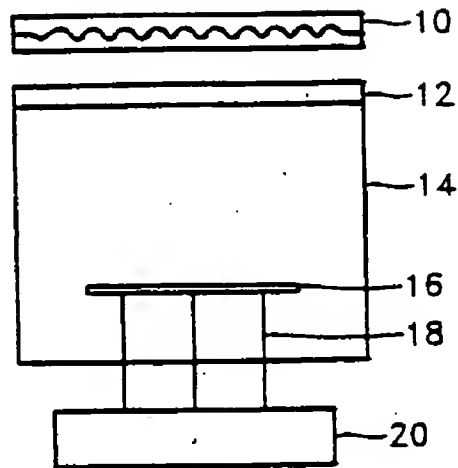


FIG. 2

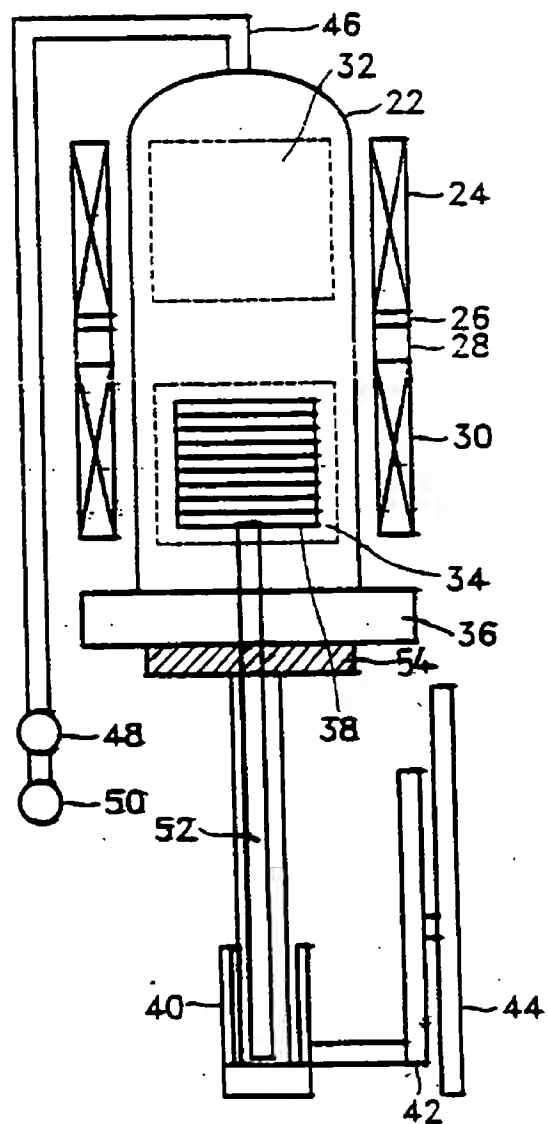


FIG. 3A

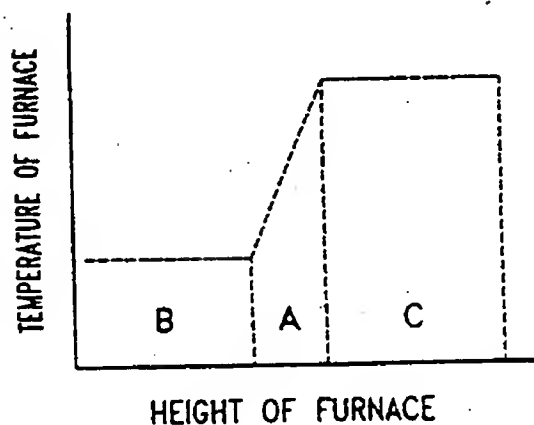
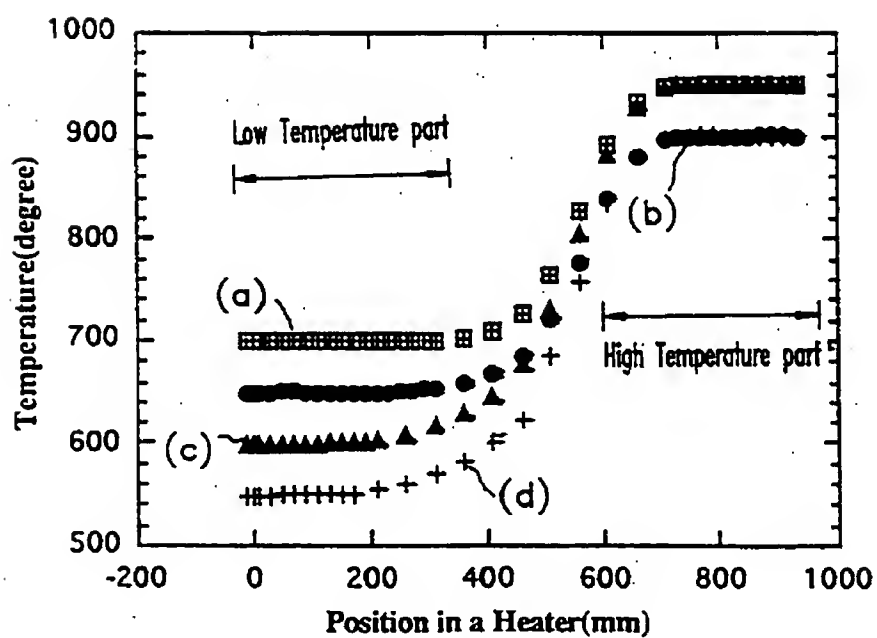


FIG. 3B



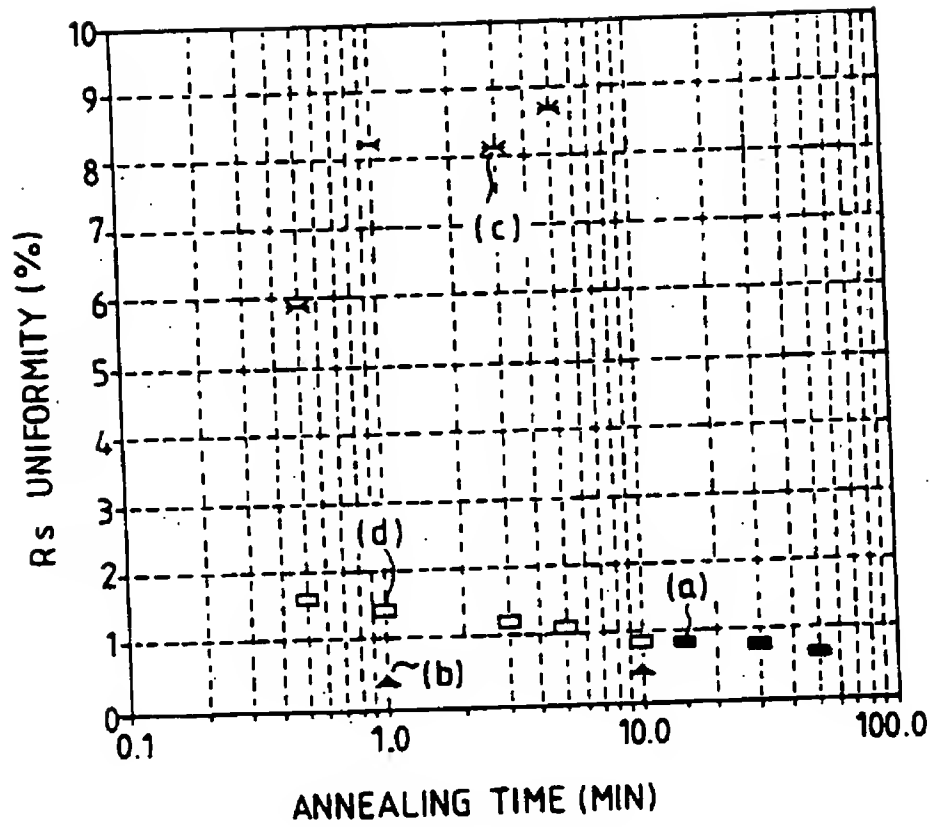


Fig.4.

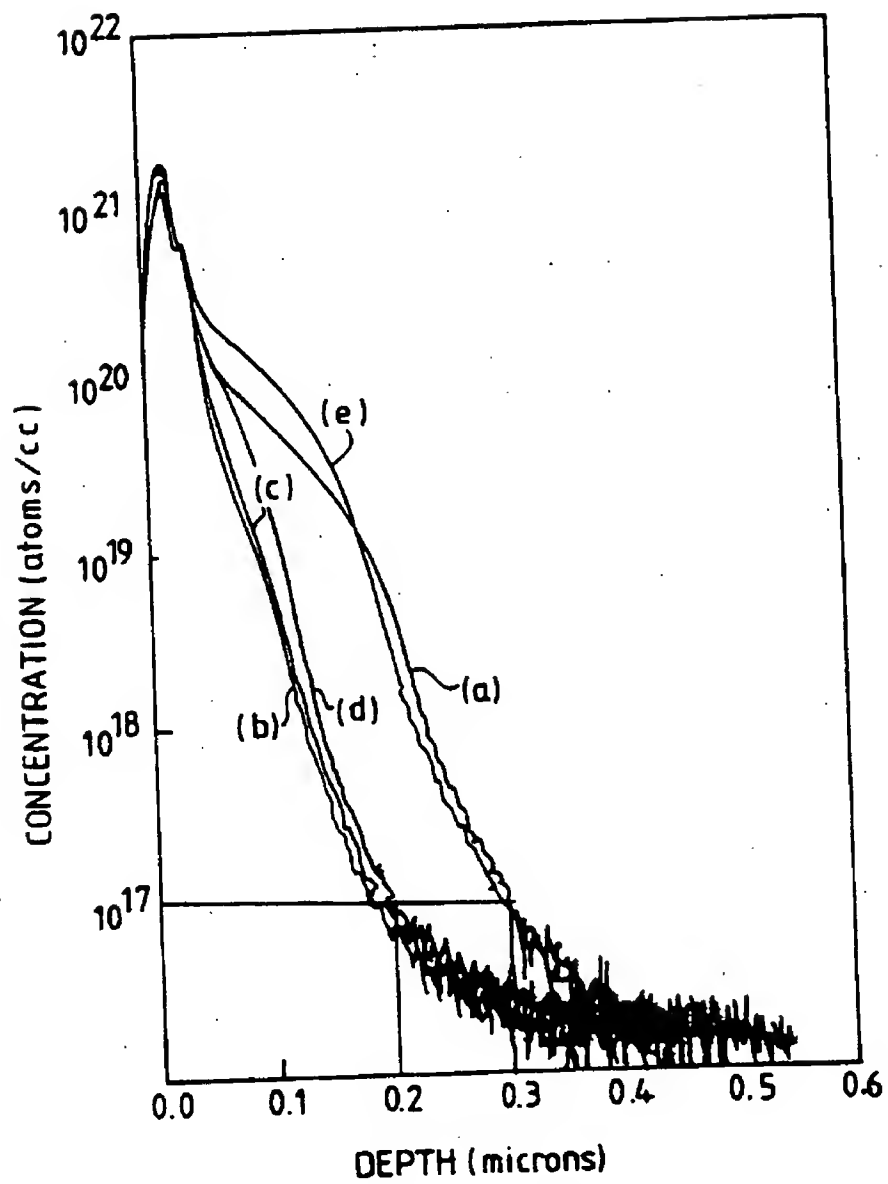


Fig.5.

METHOD AND APPARATUS FOR RAPID THERMAL PROCESSING

The present invention relates to a method and an apparatus for rapid thermal processing, and in a preferred embodiment, to a method and an apparatus for rapid thermal processing, in which a low temperature thermal processing and a high temperature thermal processing are successively performed in the same furnace.

A major advantage of rapid thermal processing (RTP) which is widely used in semiconductor device manufacturing process is to decrease the thermal budget provided to a wafer since the thermal processing is performed at a high temperature for short time using a lamp. This is in contrast with a general furnace in which the manufacturing process is performed at a low temperature for a long time, thereby increasing the thermal budget.

FIG. 1 of the accompanying drawings is a schematic diagram of an RTP apparatus according to a general lamp heating method. Here, reference numerals 10, 12, 14, 16, 18 and 20 represent a lamp heater, a quartz window, a chamber, a silicon wafer, lifter pins and a lifter assembly, respectively.

Referring to FIG. 1, quartz window 12 is mounted on chamber 14, and lamp heater 10 is located above the quartz window, maintaining a predetermined interval with respect to quartz window 12. Silicon wafer 16 is fixed by lifter pins 18 in chamber 14. Here, lifter pins 18 are controlled by lifter assembly 20. Silicon wafer 16 fixed by lifter pins 18 in chamber 14 is thermally treated by the radiant heat from lamp heater 10.

The RTP apparatus according to a general lamp heating method shown in FIG. 1 has disadvantages in that the wafer has to be thermally treated at a higher temperature than a target temperature required for the wafer, in order to achieve a high temperature

and a short heating time which are characteristics of RTP processing. Here, in order to ensure that the wafer is treated at the required temperature, a thermometer has to be set near the surface of wafer. Also, when the wafer has to be thermally treated at a temperature higher than a target temperature, the temperature read from the thermometer
5 is the temperature required.

That is, when the temperature read from the thermometer does not reach the chamber temperature, although the temperature within chamber 14 is maintained at the required temperature, the wafer is continuously thermally treated at high temperature nevertheless that the wafer is actually thermally treated at a proper temperature.

10 Furthermore, the temperature actually felt at the wafer is further increased since the silicon wafer's absorption and emission spectra do not overlap.

Also, the most significant problem due to the thermal treatment which is performed only in the upper part of chamber 14 is the generation of slip. In the case of a pattern wafer (wafer on which a pattern for manufacturing a semiconductor device is
15 formed), the temperature measured during the thermal treatment is changed according to the physical characteristics of the material constituting each layer and the temperature distribution of the wafer is uneven, thereby generating the slip at the edge of the wafer.

To overcome the generation of slip, an edge guard ring attaching method where a quartz ring of an annular shape is attached along the edge of silicon wafer or a wafer
20 rotating method where the wafer is rotated during the thermal treatment was provided. However, the above-described problems could not be solved basically.

Therefore, a new RTP apparatus which accurately thermally treats the wafer to a required temperature and evenly controls the temperature distribution within the wafer is required.

It is an object of the present invention to provide a rapid thermal processing method where the wafer is accurately thermally treated to a required temperature and the temperature distribution within the wafer can be evenly controlled.

5 It is another object of the present invention to provide a rapid thermal processing apparatus which is suitable for achieving the above object.

According to one aspect of the present invention there is provided a method for rapid thermal processing of semiconductor wafers, wherein first temperature thermal processing and second temperature thermal processing are successively performed in the same furnace, respectively in a first temperature thermal processing portion and a second
10 temperature thermal processing portion thereof, each of which being maintained at a constant temperature.

In a preferred embodiment of a rapid thermal processing method according to the present invention, low temperature thermal process is performed in a lower part of the furnace, and high temperature thermal process is performed in an upper part of the
15 furnace.

In another preferred embodiment of a rapid thermal processing method according to the present invention, the first and second temperature thermal processing portions are thermally treated by first and second heaters respectively in an annular shape surrounding the furnace. Here, the heaters adopt a resistance heating method. Also, it is desirable
20 that the first heater is thermally treated until the temperature of the high thermal processing portion reaches 400-800°C, and the second heater is thermally treated until the temperature of the low thermal processing portion reaches 600-1200°C.

According to another aspect of the present invention there is provided an apparatus for rapid thermal processing of semiconductor wafers, which comprises:

a furnace;

a first heater which is at a lower part of said furnace and has an annular shape surrounding said furnace, and

a second heater which is at an upper part of furnace directly above the first heater, and has an annular shape surrounding said furnace.

It is desirable that the rapid thermal processing apparatus further comprises an annular heat shield and a reflector between the first and second heaters.

It is desirable that the first and second heaters are thermally treated in a resistance heating method.

It is desirable that, in use, the first heater is thermally treated until the temperature of the lower part in the furnace reaches 400-800°C, and the second heater is thermally treated until the temperature of the upper part in the furnace reaches 600-1200°C.

It is desirable that the rapid thermal processing apparatus further comprises a manifold for supplying gas to the lowest part of the furnace. Here, the gas supplied to the manifold is at least one selected from the group consisting of NH_3 , N_2O , N_2 , H_2 , O_2 , Ar and He.

In the rapid thermal processing apparatus, it is desirable that, in use, the pressure of the furnace's inside is lower than an atmospheric pressure.

Therefore, according to a method and an apparatus for rapid thermal processing of the present invention, a wafer can be thermally treated in a furnace which is maintained at a constant temperature and can be thermally treated using the whole surface of the furnace. As a result, the overheating over a required temperature of the wafer can be prevented thereby decreasing the thermal budget and evenly distributing the temperature over the whole wafer, so that the generation of slip can be prevented.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG. 1 is a schematic diagram of an RTP apparatus according to a general lamp heating method;

5 FIG. 2 is a schematic diagram of a hot-wall type RTP apparatus using a resistance heating method according to an embodiment of the present invention;

FIG. 3A is a graph showing the ideal temperature profile within the furnace;

FIG. 3B is a graph showing a temperature profile in the furnace, measured through experimentation;

10 FIG. 4 is a graph showing sheet resistance uniformity in a general RTP apparatus, a general furnace and a hot-wall type RTP apparatus according to an embodiment of the present invention, and

FIG. 5 is a depth profile of boron ions, analyzed using a SIMS.

Referring to the accompanying drawings, a method and an apparatus for rapid
15 thermal processing (RTP) of a preferred embodiment according to the present invention will be explained in detail.

FIG. 2 is a schematic diagram of a hot-wall type RTP apparatus using a resistance heating method according to the present invention.

Reference numerals 22, 24, 26, 28 and 30 represent, a furnace (quartz tube), a
20 first heater, a reflector, a heat shield and a second heater, respectively. Also, reference numerals 32, 34, 36 and 38 represent an upper isothermal zone, a lower isothermal zone, a manifold and a boat, respectively. Reference numerals 40, 42 and 44 represent a magnetic coupler, a first lifter and a second lifter, respectively. Reference numerals 46, 48, 50, 52 and 54 represent an exhaust pipe, a mechanical booster pump, a dry pump, a

boat support, and a door plate, respectively.

The RTP apparatus according to this embodiment comprises furnace 22 in the shape of a capsule for thermally treating the wafer, first heater 24 which is located in the upper part of the furnace, and has an annular shape surrounding the furnace, second
5 heater 30 which is located in the lower part of the furnace, and has an annular shape surrounding the furnace, reflector 26 which is located between the first and second heaters and has an annular shape surrounding the furnace, heat shield 28 which is located between the first and second heaters and below the reflector, upper isothermal zone 32 which is located in upper part of the furnace, lower isothermal zone 34 which is located
10 in the lower part of the furnace, a manifold 36 which is located in the lowest part of furnace 22, for supplying gas to the furnace, boat 38 for carrying the wafer, first lifter 42 for lifting the boat from the lower isothermal zone to the upper isothermal zone, second lifter 44 for lifting the boat to the lower isothermal zone, magnetic coupler 40 attached to the lifters, exhaust pipe 46 connected to the uppermost part of the furnace, mechanical
15 booster pump 48 and dry pump 50 which are located on the end of the exhaust pipe, and boat support 52 for supporting boat 38.

First heater 24 can control the temperature of the furnace to 600-1200°C and second heater 30 can control the temperature of the furnace to 400-800°C. These two heaters are heated in a resistance heating method. Heat shield 28 is set for suppressing the
20 radiant heat generated between the first and second heaters. The gas supplied to the manifold is at least one selected from the group consisting of NH_3 , N_2O , N_2 , H_2 , O_2 , Ar and He, etc. Also, the pressure in the furnace is lower than atmospheric pressure.

The transportation of boat 38 is composed of two steps, as illustrated by FIG. 2. That is, second lifter 44 lifts the boat from a wafer loading position to the low

temperature thermal processing portion (lower part) of furnace and first lifter 42 lifts the boat from the low temperature thermal processing portion to the high temperature thermal processing portion (upper part). First lifter 42 is controlled to lift the boat from the low temperature thermal processing portion to the high temperature thermal processing portion at a maximum speed of 10cm/sec (0.1 ms^{-1}) and comprises magnetic coupler 40 for preventing the generation of particles in the furnace.

The wafer is lifted in furnace 22 by the operation of first and second lifters 42 and 44, while loaded on boat 38. Before the wafer is carried into furnace 22, the inside of the furnace is heated by the first and second heaters 24 and 30, thereby maintaining the required temperature. That is, the upper part of furnace is heated by the first heater to a high temperature and maintained at the high temperature. Also, the lower part of furnace is heated by the second heater to a low temperature and maintained at the low temperature. After the wafer is carried into the furnace, the gas for treating the wafer is injected and the heating is performed.

FIG. 3A is a graph showing the ideal temperature profile within the furnace, which is required in the hot-wall type RTP apparatus according to the present invention. In FIG. 3A, the horizontal axis represents the furnace height and the vertical axis represents the furnace temperature. As shown in the graph, the temperature of the furnace is classified into a high temperature part C, a transition part A and a low temperature part B. Here, the temperature of the high and low temperature parts is constantly maintained.

FIG. 3B shows the temperature profile in the furnace of the hot-wall type RTP apparatus according to an embodiment of the present invention. FIG. 3B shows the same temperature profile as that of FIG. 3A. In FIG. 3B, each line represents respectively a different furnace temperature at high temperature part/low temperature part. Lines (a),

(b), (c) and (d) represent 950°C/700°C, 950°C/600°C, 950°C/650°C and 900°C/550°C, respectively.

Therefore, according to the present invention, the wafer is treated in the furnace in which the thermal processing temperature is constantly fixed, thereby preventing the overheating of the wafer beyond a required temperature. The heater is set in a shape surrounding the furnace so that the temperature distribution of the wafer can be evenly maintained, thereby preventing the generation of slip. Also, the high and low temperature thermal treatments of the wafer can be simultaneously performed in one furnace.

FIG. 4 is a graph showing sheet resistance uniformity in a general RTP apparatus, a general furnace and a hot-wall type RTP apparatus according to an embodiment of the present invention. FIG. 4 is the result of an experiment for evaluating the uniformity of the temperature applied to the wafer during the RTP.

After the silicon wafer is oxidized to about 200Å, BF₃ ions are injected in a dose of 4.5E15 ions/cm² and at an energy of 30keV. Subsequently, after respectively thermal-processing the wafer using the general RTP apparatus, the general furnace and the hot-wall type RTP apparatus, the sheet resistance (Rs) of the silicon surface is evaluated.

In FIG. 4, line (a) is where the wafer is thermally treated at 900°C by the general furnace, line (b) is where the wafer is thermally treated at 950°C by the general furnace, line (c) is where the wafer is annealed at 950°C by the general RTP apparatus, and line (d) is where the wafer is annealed at 950°C by the hot-wall type RTP apparatus according to an embodiment of the present invention.

As shown in FIG. 4, in the case of the general RTP apparatus, the sheet resistance uniformity is 6-9%. On the other hand, the sheet resistance uniformities in the hot-wall type RTP apparatus and in the general furnace are below 2% and 1%, respectively.

FIG. 5 is a depth profile of boron ions, analyzed by a SIMS. After BF_2 ions are injected into the silicon surface in a dose of $4.5\text{E}15$ ions/ cm^2 and at an energy of 30keV , the thermal treatment is performed by the general furnace and the hot-wall type RTP apparatus. Thereafter, a junction depth is evaluated using the SIMS.

5 To provide the same sheet resistance (e.g., $R_s=145\Omega/\square$) to the silicon wafer on which BF_2 ion is injected, the silicon wafer is thermally treated, and thereafter, the junction depth of the BF_2 is measured. In FIG. 5, line (a) represents the case in that the thermal-treatment is performed at 850°C for 150 minutes in the general furnace. Lines (b), (c), (d) and (e) represent the cases in that the thermal-treatment is performed at
10 950°C for 30 seconds, at 950°C for 1 minute, at 950°C for 3 minutes and at 950°C for 10 minutes, respectively, in the hot-wall type RTP apparatus according to an embodiment of the present invention. As the result, the junction depths are of $0.32\mu\text{m}$ and $0.22\mu\text{m}$ in the cases of the general furnace and the hot-wall type RTP apparatus according to the embodiment of the present invention, respectively. Thus, it is to be understood that in the
15 case where the hot-wall type RTP apparatus according to the present invention is used, the junction depth is relatively shallow.

Therefore, according to the hot-wall type RTP apparatus of the present invention, the overheating of the wafer beyond a required temperature can be prevented, thereby decreasing the thermal budget. Also, the temperature distribution over the whole wafer
20 can be evenly maintained, thereby preventing the generation of slip. Furthermore, the hot-wall type RTP apparatus of the present invention can form a more shallow junction than with the general furnace.

While the present invention has been illustrated and described with reference to specific embodiments, further modifications and improvements will occur to those skilled

in the art. It is to be understood, therefore, that this invention is not limited to the particular forms illustrated and that it is intended in the appended claims to cover all modifications that do not depart from the scope of this invention.

CLAIMS

1. An apparatus for rapid thermal processing of semiconductor wafers, which comprises:

a furnace;

5 a first heater which is at a lower part of said furnace and has an annular shape surrounding said furnace, and

a second heater which is at an upper part of furnace directly above the first heater, and has an annular shape surrounding said furnace.

2. An apparatus for rapid thermal processing as claimed in claim 1, further comprising an annular heat shield and a reflector between said first and second heaters.

3. An apparatus for rapid thermal processing as claimed in claim 1 or 2, wherein said first and second heaters are adapted to be thermally treated in a resistance heating method.

4. An apparatus for rapid thermal processing as claimed in any of claims 1 to 3, wherein said first heater is adapted to be thermally treated until the temperature of the lower part in the furnace reaches 400-800°C, and said second heater is adapted to be thermally treated until the temperature of the upper part in the furnace reaches 600-1200°C.

5. An apparatus for rapid thermal processing as claimed in any of claims 1 to 4, further comprising a manifold for supplying gas to the lowest part of the furnace.

6. An apparatus for rapid thermal processing substantially as herein described with reference to Figure 2 with or without reference to any of Figures 3A to 5 of the accompanying drawings.

7. A method for rapid thermal processing of semiconductor wafers, wherein first temperature thermal processing and second temperature thermal processing are successively performed in the same furnace, respectively in a first temperature thermal processing portion and a second temperature thermal processing portion thereof, each of which being maintained at a constant temperature.

8. A method for rapid thermal processing as claimed in claim 7, wherein the temperature of said first temperature thermal processing portion is lower than that of said second temperature thermal processing portion.

9. A method for rapid thermal processing as claimed in claim 7 or 8, wherein said first temperature thermal processing is performed in a lower part of furnace and said second temperature thermal processing is performed in an upper part of furnace.

10. A method for rapid thermal processing as claimed in claim 7 or 9, wherein said first and second temperature thermal processing portions are thermally treated by first and second heaters each of annular shape surrounding the furnace.

11. A method for rapid thermal processing as claimed in claim 10, wherein said heaters are thermally treated using a resistance heating method.

12. A method for rapid thermal processing as claimed in claim 10 or 11, wherein said first heater is thermally treated until the temperature of the first temperature thermal processing portion reaches 400-800°C, and said second heater is thermally treated until the temperature of the second temperature thermal processing portion reaches 600-1200°C.

13. A method for rapid thermal processing as claimed in any of claims 7 to 12, wherein gas is supplied to the lowest part of the furnace and comprises at least one selected from the group consisting of NH_3 , N_2O , N_2 , H_2 , O_2 , Ar and He.

14. A method of rapid thermal processing as claimed in any of claims 7 to 13, wherein the pressure of said furnace's interior is lower than the atmospheric pressure.

15. A method for rapid thermal processing substantially as herein described with reference to Figure 2 and Figure 3A with or without reference to any of Figures 3B
5 to 5 of the accompanying drawings.

CLAIMS

1. An apparatus for rapid thermal processing of semiconductor wafers, which comprises:

a furnace;

5 a first heater which is at a lower part of said furnace and has an annular shape surrounding said furnace;

a second heater which is at an upper part of furnace directly above the first heater, and has an annular shape surrounding said furnace; and

an annular heat shield and a reflector between said first and second heaters.

10 2. An apparatus for rapid thermal processing as claimed in claim 1, wherein said first and second heaters are adapted to be thermally treated in a resistance heating method.

3. An apparatus for rapid thermal processing as claimed in claim 1 or claim 2, wherein said first heater is adapted to be thermally treated until the temperature of the lower part in the furnace reaches 400-800°C, and said second heater is adapted to be thermally treated until the temperature of the upper part in the furnace reaches 600-1200°C.

4. An apparatus for rapid thermal processing as claimed in any of claims 1 to 3, further comprising a manifold for supplying gas to the lowest part of the furnace.

20 5. An apparatus for rapid thermal processing substantially as herein described with reference to Figure 2 with or without reference to any of Figures 3A to 5 of the accompanying drawings.



Application No: GB 9605135.4
Claims searched: 1-4

Examiner: SJ Morgan
Date of search: 28 May 1996

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KLHX)

Int Cl (Ed.6): H01L

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
X	EP 0 538 874A1 (FTL) See lines 1-25, page 10	1-4

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